PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

Assistant Commissioner for Patents
United States Patent and Trademark Office
Box PCT
Washington, D.C.20231
ETATS-UNIS D'AMERIQUE

in its capacity as elected Office

Date of mailing (day/month/year) 11 August 2000 (11.08.00)	
International application No. PCT/GB99/04260	**Applicant's or agent's file reference** P20963WO9
International filing date (day/month/year) 16 December 1999 (16.12.99)	**Priority date** (day/month/year) 19 December 1998 (19.12.98)
Applicant COKER, Timothy, Martin et al	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

11 July 2000 (11.07.00)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO **34, chemin des Colombettes** **1211 Geneva 20, Switzerland**	Authorized officer Olivia RANAIVOJAONA
Facsimile No.: (41-22) 740.14.35	Telephone No.: (41-22) 338.83.38

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF THE RECORDING OF A CHANGE

(PCT Rule 92bis.1 and Administrative Instructions, Section 422)

To:

GODDARD, David, John
Harrison Goddard Foote
11C Compstall Road
Marple Bridge
Stockport SK6 5HH
ROYAUME-UNI

Date of mailing (day/month/year)
06 November 2000 (06.11.00)

Applicant's or agent's file reference
P20963WO9

IMPORTANT NOTIFICATION

International application No.
PCT/GB99/04260

International filing date (day/month/year)
16 December 1999 (16.12.99)

1. The following indications appeared on record concerning:

[ ] the applicant [ ] the inventor [X] the agent [ ] the common representative

Name and Address
GODDARD, David, John
Harrison Goddard Foote
1 Stockport Road
Marple
Stockport SK6 6BD_
United Kingdom

State of Nationality:
State of Residence:
Telephone No.: 0161 427 7005
Facsimile No.: 0161 427 7026
Teleprinter No.:

2. The International Bureau hereby notifies the applicant that the following change has been recorded concerning:

[ ] the person [ ] the name [X] the address [ ] the nationality [ ] the residence

Name and Address
GODDARD, David, John
Harrison Goddard Foote
11C Compstall Road
Marple Bridge
Stockport SK6 5HH
United Kingdom

State of Nationality:
State of Residence:
Telephone No.: 0161 427 7005
Facsimile No.: 0161 427 7026
Teleprinter No.:

3. Further observations, if necessary:

4. A copy of this notification has been sent to:

[X] the receiving Office
[ ] the International Searching Authority
[X] the International Preliminary Examining Authority
[ ] the designated Offices concerned
[X] the elected Offices concerned
[ ] other:

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No.: (41-22) 740.14.35

Authorized officer
Christine Carrié

Telephone No.: (41-22) 338.83.38

Form PCT/IB/306 (March 1994)

003636936

14

REC'D 12 MAR 2001
WIPO PCT

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
P20963WO		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/GB99/04260	16/12/1999	19/12/1998
International Patent Classification (IPC) or national classification and IPC G09G3/20		
Applicant THE SECRETARY OF STATE FOR DEFENCE et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 7 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 17 sheets.

3. This report contains indications relating to the following items:

I	☒	Basis of the report
II	☐	Priority
III	☐	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
IV	☐	Lack of unity of invention
V	☒	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
VI	☐	Certain documents cited
VII	☒	Certain defects in the international application
VIII	☒	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
11/07/2000	08.03.2001
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Morris, D Telephone No. +49 89 2399 2182

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/GB99/04260

I. Basis of the report

1. This report has been drawn on the basis of *(substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments (Rules 70.16 and 70.17).)*:
Description, pages:

1-14	as received on	05/01/2001	with letter of	05/01/2001

Claims, No.:

1-15	as received on	05/01/2001	with letter of	05/01/2001

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   - ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
   - ☐ the language of publication of the international application (under Rule 48.3(b)).
   - ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   - ☐ contained in the international application in written form.
   - ☐ filed together with the international application in computer readable form.
   - ☐ furnished subsequently to this Authority in written form.
   - ☐ furnished subsequently to this Authority in computer readable form.
   - ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
   - ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

   - ☐ the description, pages:
   - ☐ the claims, Nos.:
   - ☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

(Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	1-11
	No:	Claims	12-15
Inventive step (IS)	Yes:	Claims	1-11
	No:	Claims	12-15
Industrial applicability (IA)	Yes:	Claims	1-15
	No:	Claims	

2. Citations and explanations
see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:
see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:
see separate sheet

Re Item VIII

Certain observations on the international application

1. The following objections are made within the meaning of Article 6 PCT with respect clarity and conciseness.

1.1 The subject matter of independent claim 2 is considered obscure as, insofar as it is mentioned in said claim that "at least one said pixel [..] is brought closer to equality", the subject matter of independent claim 2 appears inconsistent with the example of the invention of page 8, fifth paragraph of the application (- as originally filed) which also mentions bringing at least one pixel further from equality (- see "grey level 16" - page 8, fifth paragraph, 3rd line) i.e. while performing time averaging of a grey level over more than one frame (- cf. page 8, fourth paragraph, lines 1-2 as originally filed), such a said inconsistency being in contravention of PCT Guidelines III-4.3.

1.1a Likewise, insofar as independent claim 14 merely mentions that the "said inequality of 1s and 0s is reduced or removed", the subject matter of independent claim 14 is also considered inconsistent with the description and, as such, is also considered obscure in the sense of PCT Guidelines III-4.3.

1.1b Furthermore it is also noted that, in some circumstances at least (- i.e. page 8, fifth paragraph as originally filed), that a feature of:

i.e. an increase of inequality of 1s and 0s in a pixel of a frame in which time averaging of a grey level is performed over more than one frame, i.e. in combination with a corresponding reduction, (- cf. page 8, fourth paragraph, lines 1-2 as originally filed),

that said such feature of at least a possibility of an increase, i.e. in combination with a reduction, would appear essential in order for the invention to be carried out, and as such failure to mention said such feature gives rise to an inconsistency in contravention of PCT Guidelines III-4.4 as not all features needed to define the invention are not clearly specified.

1.1c The term "complete image" of independent claims 2, 13 and 14 is considered obscure in the sense of PCT Guidelines III-4.2, said term:

- not having any meaning in the art;
- appearing to have a special meaning, i.e. a frame, said special meaning not being clear from the wording of the claim alone (- cf. "time averaging of both dc and grey scale level is performed over more than one frame" - page 8, lines 13-14 as originally filed); and
- appearing to have an inconsistent meaning, i.e. in present independent claims 2 and 13, the term "complete image" in each said claim appears to correspond to the features of "a frame" as mentioned in the description, whereas in present independent claim 14, the term "complete image" appears to correspond to the average of a plurality of frames i.e. "a plurality of images each approximating said complete image" (- present claim 14, line 6).

As such therefore, due to the obscurity in respect of the above term objected to, the technical sense of independent claims 2 and 13-14 is rendered obscure.

1.2 Insofar as the respective subject matters of independent claims 1 and 2 merely mention the "driving means is arranged to alter the n-bit number in respect of at least one said pixel", i.e. without clearly indicating the condition under which said alteration takes place, i.e. said at least one said binary number has an inequality of 1s and 0s (- cf. e.g. present independent claims 12-14 and independent claims 1 and 2 as originally filed), the subject matter of independent claims 1 and 2 are not considered to clearly specify all of the features essential for the invention, in contravention of PCT Guidelines III-4.4.

1.3 The term

"and so that any inequality of 1s and 0s in each of the reset of the said set of numbers is left unchanged, reduced, or removed"

of independent claims 12 and 13 is considered obscure as it is not clear from the wording of the claim alone upon what basis, if any, that "the rest of the set of numbers" (so far as understood) "is left unchanged, reduced, or removed" i.e. based merely upon the alteration of the "at least one said binary number", leading to an internal inconsistency within each of independent claims 12 and 13.

1.3a Likewise the corresponding term of independent claim 14, i.e. "and any inequality of 1s and 0s at each of the other pixels is left unchanged, reduced, or removed" is also considered obscure for reasons corresponding to those raised in the objection above against independent claims 12 and 13.

1.4 The term "set of numbers" of present independent claims 12-13 is not considered clear as it is obscure from the wording of the claims alone as to whether or not the "set" referred to comprises either:

- the n-digits in the binary number (- e.g. claim 12, line 2); or
- the set of n-digit binary number signals (- e.g. claim 12, line 2).

See in this respect "the other pixels" of the last line of independent claim 14.

1.5 The respective subject matters of independent claim 13 and 14 is considered obscure as although subject matter of each claim is claimed as being "a method of writing and displaying", no actual method steps of:

- writing,
- displaying, or i.e. even
- altering

are indicated within each of said claims, giving rise to an internal inconsistency within the respective claims, in contravention of PCT Guidelines III-4.1.

1.6 The term "drive means" of present independent claims 1 and 2 (- respective lines 6 and 7) is considered obscure as the term, as generally used in the art (- Guidelines III-4.2), is considered to imply

- the circuits used for applying respective scanning and data driving signals to pixels of the array (- cf. "adapted to drive the array" - line 2 of each of present claims 1 and 2),

whereas from what is mentioned in the last three lines of claim 1 and the last four lines of claim 2, the "drive means" (so far as understood) of each said claim appears to comprise

- e.g. an image signal processing means i.e. see "arranged to alter the n-digit number" of present claims 1 and 2 (- line 7 in each case) and "an image

signal representing a set on n-digit binary numbers" also of present claims 1 and 2 (- line 3 in each case), and also present claims 12-14 (- first line in each case).

As such there arises an internal inconsistency within each of claims 1 and 2 due to an inconsistency in respect of the meaning of the term "drive means".

Re Item V

Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

2. In respect of independent claims 12-14 and dependent claim 15, Insofar as:

- "weighted bit plane techniques" for generating images based on n-digit binary numbers are well known in the art;
- it is well known in the art, when at least one of said n-digit binary numbers has an inequality of 1s and 0s, to leave said set of numbers "unchanged" (- cf. last line of each of present claims 12-14); and insofar as
- it is well known in the art to refresh a bit plane during writing of an image,

the respective subject matters of present independent claims 12-14, and dependent claim 15, are considered to comprise no more than prior art.

Accordingly, so far as understood, the respective subject matters of independent claims 12-15 are not considered novel over known prior art within the meaning of Article 33(2) PCT.

3.1 None of the available prior art either discloses or suggests the use of an image signal processing means (so far as understood) comprising the features mentioned in the characterising portion of present independent claims 1 and 2, and as such independent claims 1 and 2 are considered to meet the requirements of novelty and inventive step (Article 33(2)(3) PCT).

3.2 Dependent claims 3-11 are also considered to meet requirements of novelty and inventive step (Article 33(2)(3) EPC).

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	FOR FURTHER ACTION	see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.
P20963WO		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/GB 99/ 04260	16/12/1999	19/12/1998
Applicant		
THE SECRETARY OF STATE FOR DEFENCE et al.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language,** the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

   [ ] contained in the international application in written form.

   [ ] filed together with the international application in computer readable form.

   [ ] furnished subsequently to this Authority in written form.

   [ ] furnished subsequently to this Authority in computer readble form.

   [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

   [ ] the text is approved as submitted by the applicant.

   [X] the text has been established by this Authority to read as follows:

MODIFIED WEIGHTED BIT PLANES FOR DISPLAYING GREY LEVELS ON OPTICAL ARRAYS

5. With regard to the **abstract,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. –

   [ ] as suggested by the applicant.

   [ ] because the applicant failed to suggest a figure.

   [ ] because this figure better characterizes the invention.

   [X] None of the figures.

INTERNATIONAL SEARCH REPORT

International Application No
P[redacted]GB 99/04260

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G09G3/20 G09G3/34

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 720 139 A (PIONEER ELECTRONIC CO.) 3 July 1996 (1996-07-03) see abstract page 2, line 5 -page 3, line 15; figures 1-3,22-24 page 3, line 54 -page 5, line 46	1,2,6
A	US 4 775 891 A (AOKI ET AL.) 4 October 1988 (1988-10-04) see abstract column 3, line 4 -column 5, line 58; figures 1-5	2,3

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
2 May 2000	09/05/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Corsi, F

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Form PCT/ISA/210 (second sheet) (July 1992)

International Application No
P[redacted]B 99/04260

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 17, no. 498 (P-1609), 8 September 1993 (1993-09-08) -& JP 05 127612 A (NIPPON HOSO KYOKAI), 25 May 1993 (1993-05-25) abstract	2
A	EP 0 774 745 A (MATSUSHITA ELECTRONICS CO.) 21 May 1997 (1997-05-21) see abstract column 3, line 14 -column 5, line 14; figures 36-40 column 6, line 34 - line 57; figure 44 column 8, line 9 - line 19 column 12, line 9 -column 13, line 14; figures 1-3 column 25, line 12 -column 27, line 13; figures 26-30	6

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
P[redacted]B 99/04260

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 720139 A	03-07-1996	JP 8234694 A	13-09-1996
		JP 9102921 A	15-04-1997
		US 6025818 A	15-02-2000
US 4775891 A	04-10-1988	JP 1926656 C	25-04-1995
		JP 6057059 B	27-07-1994
		JP 61234673 A	18-10-1986
		JP 1934237 C	26-05-1995
		JP 6057058 B	27-07-1994
		JP 61060089 A	27-03-1986
		DE 3531210 A	13-03-1986
		GB 2164190 A,B	12-03-1986
JP 05127612 A	25-05-1993	NONE	
EP 774745 A	21-05-1997	JP 9198006 A	31-07-1997
		US 5940142 A	17-08-1999

MODIFIED WEIGHTED BIT PLANES FOR DISPLAYING GREY LEVELS ON OPTICAL ARRAYS

The present invention relates to methods of operating a display or spatial light modulator in which the instantaneous intensity distribution afforded by the display or modulator is binary in nature but which is altered in a manner such that the time averaged distribution effectively has, or appears to have, multiple intensity levels. For display purposes, this means that the alteration must be sufficiently fast for averaging to occur at the eye, preferably avoiding any flicker. This requirement may or may not apply for other purposes.

The invention can be used in conjunction with any spatial light modulator capable of producing a binary image, including those comprising an array of individually addressable cells or pixels, and those where the binary image is produced by scanning of a modulated light beam, for example. The term " binary spatial light modulator " used herein is intended to encompass all such devices, whether they are used for display or other purposes, for example information recordal, and variable components (for example lenses, filters and diffraction gratings) in optical systems. The term is intended to cover passive modulators where an existing light beam is affected by the modulator, and also those which act as light sources, for example arrays of light emitters, and electroluminescent devices.

The term "image" as used herein is used to denote any spatially varied light distribution, normally, but not necessarily, of light intensity, and its production or resulting distribution will be referred to by the term "display".

Furthermore, although the term "grey scale" is used herein as denoting a multi-level distribution, it should be made clear that the term is used in relation to any colour, including white. In addition, although the methods, arrays, backplanes, circuitry etc. of the invention and its embodiment are described in relation to a single colour (monochrome images), including white, it is envisaged that variable colour images or

displays etc. will be produced in manners known per se, such as by spatially subdividing a single array into different colour pixels, superimposing displays from differently coloured monochrome arrays for example by projection, or temporal multiplexing, for example sequential projection of red green and blue images.

Temporally varying binary modulation to achieve a multiple intensity effect is known, and can be effected by the use of multiple bit planes. In such a scheme, an array of digitised values, of amplitudes corresponding to the grey scale values allocated to the pixels of the array, is decomposed into a multiplicity of bit planes. This multiple bit plane technique may be used with any binary spatial light modulator as defined above.

It is possible to decompose a n-level grey scale image into a plurality of binary image planes of equal duration, with a corresponding plurality of bitplanes of equal duration. However, in a preferred form, known as a weighted bit plane technique, the durations of the bit planes are weighted, each bitplane being representative of one level (exponent) of the digitisation. This reduces the number of bit planes required to synthesise an image, and reduces addressing requirements somewhat.

Although in certain cases, it would be possible to use digital bases other than 2, this complicates matters insofar as each bit plane is not binary and thus is not so easily stored. Furthermore, each location of such a bit plane would then have more than one non-zero value, and the variation in non-zero values across the bit plane would need to be taken into account for the durations of operation of each pixel (possibly by further decomposing the non-binary plane to two or more binary planes). The discussion below will be limited to binary weighting, but the principles set out in such a context are believed to be sufficient to enable the skilled person to extrapolate to other exponential bases if required or desired.

Where the digitisation is binary, so that each bit plane is an array of digital 1s and 0s, it is then only necessary to display each bit plane for a total period proportional to its

binary weighting to provide a time averaged image equivalent to the digitised grey scale image.

Where possible, it is convenient to display each binary bit plane once for the total duration necessary to contribute to the grey scale image, but it is also possible to display one or more of the bit planes a plurality of times, not necessarily sequentially, provided that the total time spent in displaying each bitplane, relative to the total time spent in displaying all the bitplanes, is proportional to its binary weighting.

Recently there has been developed a novel spatial light modulator in the form of a smectic liquid crystal layer disposed between an active semiconductor backplane and a common front electrode. It was developed in response to a requirement for a fast and, if possible, inexpensive, spatial light modulator comprising a relatively large number of pixels (320 x 240 up to 640 x 480) with potential application not only as a display device, but also for other forms of optical processing such as correlation and holographic switching. Depending on the manner in which it is driven, and the value of the applied voltage, the modulator may be driven at a line rate of at least 10MHz and a frame rate of up to 15 to 20kHz, requiring a data input of around 1 to 1.5 Gpixel per second. Typically, while the pixel address time is around 100 nanoseconds, the pixel will actually take around 1 to 5 microseconds to switch between optical states; and while overall frame writing time is of the order of 24 microseconds, the frame to frame writing period is around 80 microseconds.

This spatial light modulator can be driven according to single pass schemes, in which the front electrode is placed at a potential of V/2 relative to the backplane pixels, which are switched to zero volts or V volts.

Alternatively it can be driven according to double pass schemes in which in one pass the front electrode is placed at zero volts and selected pixels are turned ON by switching pixel elements of the backplane array to V volts, and in the other pass the front electrode is placed at V volts and selected pixels are turned OFF by switching elements of the array to zero volts. For pixels which are not in the process of being

switched the elements of the backplane follow the voltage of the front electrode. To maintain the same potential difference therebetween, the voltage at all backplane pixel elements of the array is simultaneously switched as the voltage on the front electrode is changed between zero and V volts.

Our copending International Patent Applications (ref: P20957WO, priority GB9827952.4; P20958WO and P20958WO1, both priority GB9827965.6; P20959WO, priority GB9827900.3; P20960WO, priority GB9827901.1; P20961WO, priority GB9827964.9; P20962WO, priority GB9827945.8; and P20963WO1, priority GB9827944.1) relate to other inventive aspects associated with this spatial light modulator, including the single and double pass schemes referred to in the preceding paragraph.

The aforesaid spatial light modulator is ideally suited to the use of the bitplane technique mentioned above. However, the present invention is not limited to liquid crystal modulators, but can be applied to any spatial light modulator as referred to above.

One problem which arises, particularly when operating liquid crystal display and modulators, is that of maintaining a dc balance at individual pixels. Initially, liquid crystal light modulators were in the form of a single cell comprising a layer of liquid crystal material sandwiched between opposed electrode bearing plates, at least one of the plates being transparent. Such cells were slow to operate and tended to have a short life due to degradation of the liquid crystal material. Quite early on it was recognised that the application of an average finite dc voltage to the liquid crystal cell was not beneficial, and at least in some cases produced degradation by electrolysis of the liquid crystal material itself, and schemes were evolved to render the average dc voltage to zero (dc balance).

It is now appreciated that other effects are also at work when a dc voltage is applied. When driving liquid crystal electro-optic devices for any length of time, a phenomenon known as image sticking may occur. Although the precise cause of this

effect is unknown, there are theories that ions are trapped or a space charge is induced within the material in response to an overall dc field, and this results in a residual field even when the external dc field is removed.

It is evidently desirable that the time averaged voltage (that is, the average over the time that the voltage is actually being applied from an external source to the liquid crystal) applied to a liquid crystal material is zero, whether to avoid degradation or to avoid image sticking.

The present invention is directed to a weighted bit plane technique as described above in which at least some of the bit planes are modified. It has particular but not exclusive relevance to the production of effective grey scale intensity distributions for display purposes, where the effective duration of the binary images (length and/or number of repeats) is such that temporal integration thereof, for example by a viewer, gives the grey scale image. It finds particular but not exclusive application to liquid crystal spatial light modulators.

The different bit planes for a grey scale image can be stored as sequential binary strings in a computer, and will be read out one at a time in any desired order after which they can be discarded unless the image needs to be repeated. It is computationally easiest to read out the bit planes in the order in which they have been stored, since then the only address which needs to be stored is the starting address of the first stored bit planes, all bit planes then being read out one at a time simply by clocking out a predetermined number of data bits in sequence for each bit planes.

It might be possible immediately to replace bit planes that have been read by the bit planes for a succeeding image, particularly where the bit planes are being produced in real time. However, under other circumstances this could be difficult, and the set of bit planes for a successive image will then normally be stored elsewhere. In certain cases it would be possible to provide storage for just two bit planes one of which is written while the other is being read, and vice versa.

It would also be possible to control the reading and/or writing processes so as to convert the image standards as desired, for example from line sequential to interlaced.

As or after each bit plane is read from memory, it is then written, e.g. using the single pass scheme described above, and viewed over a period corresponding to its weighting so that the eye synthesises the intended grey scale image. The single pass scheme is preferred insofar as it merely over-writes the preceding bit frame without the need for a second pass, the associated front electrode switching and blanking pulses. The avoidance of lost time between successive valid images enables continuous illumination and the easier provision of bit frames of an accurately weighted duration.

In such a scheme, each pixel is subjected to a series of voltage pulses according to the point in the grey scale it represents (as in the number representing the grey scale level, and usually but not necessarily in that order). There are more points in the grey scale than there are applications of voltages, due to the weighting employed, which is advantageous since it reduces the time spent actually driving the array. Each applied voltage may be of the same or opposed polarity compared to the preceding voltage, and the same number of voltage pulses, equal to the number of bit planes (ignoring polarity), is applied to each pixel to synthesise the image.

For example, in a 64 level grey scale with binary weighting, there will be 6 bit planes with relative durations of $2^n t$ where n ranges from 0 to 5, and each pixel can be represented by a corresponding 6 digit binary number.

However, double pass schemes could alternatively be adapted for use in multiple or weighted bit plane schemes.

To achieve dc balance, it would be possible to produce each binary bit plane by any binary imaging method which itself produces dc balance - for example by starting from a blank image, writing, viewing and erasing the binary image by selective energisation (+V) and driven blanking (-V) of selected pixels only.

However, in most or all of such schemes, the actual duration of the binary image is not directly proportional to the time allocated thereto, for example because of intervening blanking steps, etc., leading to a degree of distortion in the binary nature of the bitplane periods, and hence the perceived grey scale values. While this could be compensated for if desired, it represents an additional complication.

The present provides multiple or weighted bit plane schemes in which dc balance is approached or achieved in ways other than by employing dc balanced binary images per se.

For any selected pixel, each grey scale level can be represented by a binary number, and there are certain binary numbers which possess equal numbers of 0 and 1 digits, for example 111000 and 010101. In these cases the average dc voltage over the 6 bit planes will be zero. Other binary numbers, such as 011000 and 010001 come close to this ideal, and others, in particular 111111 and 000000 are far removed therefrom.

Thus to achieve dc balance in such a scheme, another possibility is (a) to use only those numbers which by themselves achieve dc balance, or (b) at least to alter the grey scale numbers to closely adjacent numbers which closely approach dc balance. This permits use of a single or double pass scheme (see above, and also our copending applications P20961WO and 20962WO), addressing all elements during each scan. Some of these schemes per se normally provide no inherent dc balance, and yet in this case dc balance or at least an approximation thereto can be obtained over the grey scale imaging time.

In the first instance (a), where the desired grey level differs, it is approximated by the nearest such number in value, for example 000110 becomes 000111, and 100010 becomes 100011. A drawback is that there can be significant distortion of the greyscale.

In the second instance (b), distortion of the greyscale can be reduced but at the expense of precise dc balance. For example, the number 001000 may become 001001, and 110111 may become 110110.

In either instance, unless further corrective steps are taken, extreme values of the grey scale will be omitted (e.g. replaced by an adjacent less extreme value), thus reducing or compressing the contrast range somewhat.

Accordingly, the invention provides a method of grey scale imaging using a weighted bit plane technique, in which an n-digit binary number represents the intended grey level of each pixel location in an array of binary pixels, wherein at least one said binary number has an unequal number of 1s and 0s, said method comprising the step of altering the number to a closely adjacent value such as to reduce the inequality of 1s and 0s (single image method)

In a refinement, time averaging of both dc and grey scale level is performed over more than one frame, by suitable choice of the binary numbers. In this manner, dc balance can be closely approximated, or preferably attained, while the average grey scale level can be approximated or, preferably, maintained. For example, 110110 (27) could be replaced by 001110 (28) in a first frame and by 010110 (26) in second frame. The average grey scale level is 27 as desired, and both the binary numbers actually used provide dc balance per se.

In a more complicated example, the grey scale level 15 (111100) could be used twice together with an additional frame for grey level 14 (011100) and another additional frame for grey level 16 (000010), the frames in any desired order. Over the four frames the average grey level is 15, and there are equal numbers of binary 1s and 0s.

Accordingly, the invention also provides a method of writing and displaying a grey scale image using a weighted bit plane technique, in which an n-digit binary number represents the intended grey level of each pixel location in an array of binary pixels, wherein at least one said binary number has an unequal number of 1s and 0s, in which

a plurality of images approximating said grey scale image are written in succession, said method comprising the step of altering the number to closely adjacent values over said plurality of images such as to reduce the inequality of 1s and 0s (plural image method). Preferably the inequality is eliminated. The grey scale as measured over the plurality of images is at least approximated, but preferably maintained.

Again extremes of the grey scale are preferably omitted. If in either case, the full grey scale ranges are retained, dc balance can be periodically restored by other means, for example by applying corrective dc pulses as appropriate following a computer simulation of the dc imbalance which has accumulated, as mentioned above. However, this is not normally preferred, since it potentially involves using a number of corrective dc pulses equal in number to the number of bit planes which have been used, to allow for the possibility that at least one pixel has remained at an extreme grey scale value throughput the imaging period.

These ways of maintaining dc balance in grey scale imaging arise at least in part from the reduction in number of address steps compared with the number of grey scale levels. One way of deriving the grey scale value or combinations of grey scale values for use in operation of the multiple or weighted bit plane scheme, that is, replacing the input grey scale value derived from the intended image itself, is by means of a look-up table.

The weighted bitplane method as operated above does require that relaxation of the liquid crystal pixels is negligible over the duration of the longest bitplane, and this is not always possible. In such a case, the bitplanes can be refreshed during the bitplane period(s), but at the possible expense of dc balance. Nevertheless there are advantages in the ease of obtaining an accurately simulated grey scale.

Basically, a refresh step comprises repeating the application of the same voltage as was applied at the start of the bitplane so as to restore the switched state of the pixel. It may even be that the nth power binary weighted bitplane needs to be refreshed (2^n-1) times subsequent to the first writing so that a 2^n greyscale will involve 2^n frame

writes of binary images when the refresh writing stages are included. However, the increasing number of writing steps makes it increasingly difficult to alter the bit frames according to the invention in the direction of providing dc balance, and in the limit of 2^n frame writes, the present invention cannot be successfully applied.

However, there will be occasions where refreshing is only necessary with the longer duration bitplanes. In such a case it would be again be possible to practice a method according to the present invention, using the actual binary numbers describing the pixel as previously described. However, a preferred method according to the invention is practised by taking determining the aggregate of the 1s and 0s occurring over the whole frame (single image method) or frames (plural image method), including the refreshed values, and altering the number for a pixel having an inequality of 1s and 0s so determined as to reduce the inequality. That is, that this preferred method acts on the binary numbers for each pixel as expanded according to the need to refresh.

For example, taking a simple example of pixels represented by a binary number comprising only four digits pixel, where the first two, higher order, digits need to be refreshed, but the 3rd and 4th can be displayed without the need to refresh, it will ne necessary to refresh the longest bit plane four times and the next longest twice. Taking the number 1001, this then becomes (1111)(00)01, where the brackets demarcate the original digits, having 5 unit values but only three zeros. Conversion of the original number to 1000 gives equality of values in the expanded number (11110000).

In the refresh scheme, bitplanes are read out more than once, depending on the duration thereof. Thus it is not possible to discard the bitplane until it has undergone its final reading. Furthermore, if each bitplane is repeatedly read for the requisite number of times before proceeding to the next bitframe, it is necessary to store the starting address of the two bitplanes.

For example, taking a simple case of three bitplanes A, B and C, of relative durations 4t, 2t and t respectively, it would be possible to read these out in the order AAAABBC. However, this necessitates storing the start addresses of each of the bitplanes, apart from frame C which is read only once, in order that the correct place for the refresh readout may be reached.

In addition, and perhaps more importantly, there are cases where it is necessary to rewrite the entire grey scale image before proceeding to a new image, where display times are long or relaxation is fast for example. In such a case it is necessary not only to store the start address of the bitplane next to be used, but also the start address of the first bit plane of the entire sequence, until that image information is no longer required.

An improved method of readout in such cases makes it possible to avoid the storage of a plurality of start addresses. At the high speeds involved in reading out the images when using the spatial light modulator of the preferred embodiment, this apparently minor step can be computationally significant and advantageous.

Essentially, a plurality of the highest order bitplanes (or all the bitplanes), are stored as binary strings in sequential locations in a memory, in decreasing order of intended duration (weighting), a predetermined number of read passes are made from the set of stored bitplanes equal to the plurality of weighted bitplanes, each pass commencing with the highest order bitplane and continuing along the stored bitplanes in sequence, the lengths of the sequences being selected and varied such that at the end of the predetermined number of read passes each bit frame has been read out a plurality of times proportional to or equal to its duration (weighting). This general method of fast readout forms the subject of our copending International Patent Application (ref: P20963WO1) filed on the same day as this application.

Thus according to this scheme, the triple bitframe image exemplified above will be read out with read passes ABC (once), AB (once), and A (twice), which when combined can give an overall order, for example, of ABCABAA, or ABCAAAB or

ABAAABC as desired. Only the start address needs to be stored since each read pass commences at the same place, and continues to an address determined by counters.

Where grey scale imaging is practised according to the invention, but with refreshing of a plurality of the highest order bitplanes, it is possible to apply this fast readout method to the set comprising the bitplanes which are refreshed plus the next lowest order bitplane. Any remaining lower order bitplane(s) which are not refreshed will be read out once, for duration(s) less than the lowest order bitplane of the set according to their weighting. This can be done at any time, including a period or periods within the reading out of the plurality, but is preferably performed before or after the entire set has undergone a fast readout.

While some of the grey scale and refresh schemes above automatically provide dc balance, a further option for schemes which do not do this is to allow dc imbalance to accumulate, for example while writing images and then allowing them to relax, calculating the imbalance (e.g. in an accompanying computer simulation), and then applying local dc voltages to the pixels of a magnitude and duration such as to provide zero average dc.

It should be understood that there have been references above to a liquid crystal cell incorporating an addressable array, the methods of the invention may be used in relation to any binary spatial light modulator. Where the imaging device is a liquid crystal device, prolongation of the binary images used to synthesise the grey scale image may be achieved in known manner by the application of an ac field between successive binary images.

CLAIMS

1. A method of grey scale imaging using a weighted bit plane technique, in which an n-digit binary number represents the intended grey level of each pixel location in an array of binary pixels, wherein at least one said binary number has an unequal number of 1s and 0s, said method comprising the step of altering the number to a closely adjacent value such as to reduce the inequality of 1s and 0s.

2. A method of writing and displaying a grey scale image using a weighted bit plane technique, in which an n-digit binary number represents the intended grey level of each pixel location in an array of binary pixels, wherein at least one said binary number has an unequal number of 1s and 0s, in which a plurality of grey scale images each approximating said grey scale image are written in succession, said method comprising the step of altering the number to closely adjacent values in at least one of said plurality of images such as to reduce the inequality of 1s and 0s.

3. A method according to claim 2 wherein said values of said number over said plurality of images provide an average grey scale level equal to the intended grey scale level.

3. A method according to any preceding claim wherein said inequality of 1s and 0s is reduced to zero (equality).

4. A method according to any preceding claim wherein said number is altered according to data in a look-up table.

5. A method which is a modification of the method according to any preceding claim wherein at least the highest order bitplane is refreshed, wherein the determination of the inequality takes into account the number of times each bitplane is refreshed.

6. A method which is a modification of the method according to any preceding claim wherein a plurality of the highest order bitplanes are refreshed, said plurality plus the next highest bitplane constituting a set, in which said set of bitplanes are stored as binary strings in sequential locations in a memory, in decreasing order of intended duration (weighting), a number of read passes equal to said plurality are made from the set of stored bitplanes, each pass commencing with the highest order bitplane and continuing along the stored bitplanes in sequence, the lengths of the sequences being varied and selected such that at the end of the said number of read passes each bit plane has been read out a plurality of times proportional to or equal to its duration (weighting).

7. A method according to claim 6 wherein said set is all of the bitplanes.

8. A method according to claim 6 wherein there is at least one additional lower order bitplane which is read out once, for a duration less than the duration of the lowest order bitplane of said set according to its weighting.

9. A method according to any one of claims 6 to 8 wherein the said number of read passes is repeated.

10. A method according to any preceding claim when used to address a spatial light modulator in the form of a liquid crystal display.

11. A method according to any preceding claim wherein a small ac potential difference is applied to pixels of the array in periods when images are not being written.

INTERNATIONAL SEARCH REPORT

Int[redacted]al Application No
PCT/GB 99/04260

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G09G3/20 G09G3/34

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 720 139 A (PIONEER ELECTRONIC CO.) 3 July 1996 (1996-07-03) see abstract page 2, line 5 -page 3, line 15; figures 1-3,22-24 page 3, line 54 -page 5, line 46	1,2,6
A	US 4 775 891 A (AOKI ET AL.) 4 October 1988 (1988-10-04) see abstract column 3, line 4 -column 5, line 58; figures 1-5	2,3

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
2 May 2000	09/05/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Corsi, F

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 17, no. 498 (P-1609), 8 September 1993 (1993-09-08) -& JP 05 127612 A (NIPPON HOSO KYOKAI), 25 May 1993 (1993-05-25) abstract	2
A	EP 0 774 745 A (MATSUSHITA ELECTRONICS CO.) 21 May 1997 (1997-05-21) see abstract column 3, line 14 -column 5, line 14; figures 36-40 column 6, line 34 - line 57; figure 44 column 8, line 9 - line 19 column 12, line 9 -column 13, line 14; figures 1-3 column 25, line 12 -column 27, line 13; figures 26-30	6

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/GB 99/04260

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 720139 A	03-07-1996	JP 8234694 A	13-09-1996
		JP 9102921 A	15-04-1997
		US 6025818 A	15-02-2000
US 4775891 A	04-10-1988	JP 1926656 C	25-04-1995
		JP 6057059 B	27-07-1994
		JP 61234673 A	18-10-1986
		JP 1934237 C	26-05-1995
		JP 6057058 B	27-07-1994
		JP 61060089 A	27-03-1986
		DE 3531210 A	13-03-1986
		GB 2164190 A,B	12-03-1986
JP 05127612 A	25-05-1993	NONE	
EP 774745 A	21-05-1997	JP 9198006 A	31-07-1997
		US 5940142 A	17-08-1999